selectively activates at least some of the plurality of independent clock signals in response to received condition data during an active mode.

7. (Once Amended) The circuit of claim 1 wherein the memory clock tree circuit includes a plurality of logic circuits, wherein each logic circuit outputs one of the plurality of corresponding independent clock signals and wherein each logic circuit is coupled to operatively receive different condition data associated with different condition data sources.

8. (Twice Amended) A power consumption reduction circuit comprising:

a memory clock source for a graphics controller;

a memory clock tree circuit, operatively coupled to the memory clock source, that generates branches of memory clock output signals as a plurality of corresponding independent clock signals to a number of memory interface circuits for differing processing engines and selectively activates at least some of the plurality of independent clock signals in response to received condition data;

an engine clock source operatively coupled to a switching circuit that generates an output engine clock signal that is selectively coupled as a clock signal to each of a plurality of registers associated with at least one of: a video overlay engine, a video capture engine, I2C control logic and a multimedia port, such that the switching circuit disables the output engine clock signal in response to receiving condition data; and

a plurality of memory read latch circuits and a memory read latch control circuit operative to dynamically activate and de-activate the plurality of memory read latches based on detected memory read requests to facilitate memory access activity based power reduction.

12. (Once Amended) The circuit of claim 8 wherein the memory clock tree circuit includes a plurality of logic circuits, wherein each logic circuit outputs one of the plurality of corresponding independent clock signals and wherein each logic circuit is coupled to operatively receive different condition data associated with different condition data sources.

13. (Twice Amended) A power consumption reduction method comprising:

generating branches of memory clock output signals as a plurality of corresponding independent clock signals to a number of memory interface circuits for differing processing engines;

selectively activating at least some of the plurality of independent clock signals in response to received condition data;

selectively coupling an engine clock signal to each of a plurality of registers associated with at least one of: a video overlay engine, a video capture engine, I2C control logic and a multimedia port to selectively disable the output engine clock signal in response to receiving condition data; and

dynamically activating and de-activating a plurality of memory read latches based on detected memory read requests to facilitate memory access activity based power reduction.

16. (Once Amended) The method of claim 13 including:

outputting one of the plurality of corresponding independent clock signals from a different branch circuit based on receiving different condition data associated with different condition data sources.

17. (New) The circuit of claim 1, wherein the received condition data includes at least one of: CRT controller enable data, GUI active condition data, GUI write condition data, scaler enable data, sub-picture "on" data, video capture enable data, half frame buffer data, and scaler enable data.

18. (New) The circuit of claim 8, wherein the received condition data includes at least one of: CRT controller enable data, GUI active condition data, GUI write condition data, scaler enable data, sub-picture "on" data, video capture enable data, half frame buffer data, and scaler enable data.

19. (New) The method of claim 13, wherein the received condition data includes at least one of: CRT controller enable data, GUI active condition data, GUI write condition data, scaler enable data, sub-picture "on" data, video capture enable data, half frame buffer data, and scaler enable data.